REMARKS

Claims 1 – 34 are pending. Claims 1, 4, 11, and 15 are currently amended, and claims 28 – 34 are new. As discussed below, the claims are in condition for allowance. **But if after considering this response the Examiner does not agree that all of the claims are allowable, he is respectfully requested to schedule and conduct a telephone interview with the Applicants' attorney before issuing a subsequent Office Action.**

Interview Summary

The Applicants' attorney thanks the Examiner and his supervisor for partaking in a phone interview with the Applicants' attorney and coinventor Mr. John Rapp on September 07, 2006. During the phone interview, the Examiner and his supervisor agreed in principle that the above amendments to the claims overcome the art-based rejections for reasons discussed below. The Examiner and his supervisor also agreed to remove the 112 rejection if the Applicants' attorney identifies support of the rejected claims in the specification, which the Applicants' attorney has done below.

Rejection of Claims 1-3, 5-10, and 15-22 Under 35 U.S.C. § 112, First Paragraph

Claim 1 as amended recites a plurality of pipeline units each comprising a respective hardwired-pipeline circuit that is coupled to receive a respective clock signal that is unsynchronized with the respective clock signal received by at least one of the other hardwired-pipeline circuits.

During the interview and in the Office Action, the Examiner expressed confusion as to how the clock signals to the hardwired-pipeline circuits could be unsynchronized in view of the SYNC signals provided to the pipeline units, *e.g.*, in FIGS. 4-8 of the patent application. This is explained below, and specification support for the amendment to claim 1 is identified.

Referring to paragraph [57] of U.S. Publication No. 2004/0136241, which was filed on the same day as, and is incorporated by, the present patent application, the

pipeline units 78 (*e.g.,* FIG. 6 of the present application) are "peers" that can communicate directly within one another, *e.g.*, via a communication bus 94 (*e.g.*, FIG. 6 of the present application).

Referring to FIGS. 4-5 and paragraph [71] of U.S. Publication No. 2004/0136241, each pipeline unit 78 includes a pipeline circuit 80, which receives a respective CLOCK signal that is separate and distinct from the SYNC signal. As discussed with the Examiner and in, *e.g.*, paragraphs [78] – [81] of the present application, the SYNC signal is not a clock signal, but acts like a "handshake" between peers to indicate, for example, that a peer has sent or received a block of data.

Referring to, *e.g.,* paragraphs [73] – [74] of U.S. Publication No. 2004/0136241, the pipelines 74 within a pipeline circuit 80 of a pipeline unit 78 can operate simultaneously and asynchronously relative to another peer, such as another pipeline unit 78, thus indicating that the respective CLOCK signals may be unsynchronized with one another, *i.e.*, may be derived from respective independent sources.

The specification supports claims 2-3, 5-10, and 15-22 for similar reasons.

Rejection of Claim 4 Under 35 U.S.C. § 103(a) In View of U.S. 6,282,627 To Wong

Claim 4

Claim 4 as amended recites that each hardwired-pipeline circuit is disposed on a respective field-programmable-gate–array die.

For example, referring, *e.g.*, to FIGS. 5-6 of the present application, each of the hardwired-pipeline circuits 80 may be disposed on respective field-programmable-gate-array dies.

In contrast, not only does Wong teach away from disposing hardwired-pipeline circuits on multiple FPGA dies, Wong does not suggest this even if the teaching away is disregarded.

Regarding the teaching away, col. 1, lines 52-54, col. 2, lines 48-50, and col. 5, lines 40-43 include but a few of the disparaging remarks Wong makes about FPGA technology (*i.e.*, the configurable architecture within an FPGA). Furthermore, nowhere does Wong temper these remarks by, for example, stating or suggesting that FPGA technology may be suitable for use in his architecture.

Furthermore, disregarding Wong's teaching away for the moment, even if it were obvious to replace Wong's DPUs (FIG. 6) with FPGA technology, it would not be obvious to replace the DPUs with respective FPGA dies. The Examiner seems to be confusing FPGA technology with FPGA dies. Wong discloses a single-die (*i.e.*, monolithic), not a multi-die, architecture. Therefore, although it may be trivial to replace the coarse-grained technology in each of Wong's DPUs with an FPGA's fine-grained technology (*e.g.*, col. 5, lines 30-42), it is impossible to replace Wong's DPUs with respective FPGA dies. And an argument by the Examiner that it would be obvious to scale Wong's single-die architecture to a multi-die architecture so that one can replace the DPUs with FPGA dies would fail, because such scaling is not trivial, and Wong fails to teach or suggest how to perform such scaling or provide a reasonable expectation that such scaling would be successful.

Rejection of Claims 1-3 and 5-27 Under 35 U.S.C. § 103(a) As Being Unpatentable Over Wong In View of U.S. Patent 6,023,742 to Ebeling

As discussed below, the Applicants' attorney respectfully disagrees with this rejection.

Claim 1

Claim 1 as amended recites a plurality of pipeline units each comprising a respective hardwired-pipeline circuit that is coupled to receive a respective clock signal that is unsynchronized with the respective clock signal received by at least one of the other hardwired-pipeline circuits.

For example, referring, e.g., to FIGS. 4-5 and paragraph [71] of U.S. Publication No. 2004/0136241, which the present application incorporates by reference, each pipeline unit 78 includes a pipeline circuit 80, which receives a respective CLOCK signal (that is separate and distinct from the SYNC signal), and that may be unsynchronized with another CLOCK signal received by at least one of the other pipeline circuits 80.

In contrast, Wong does not disclose pipeline units each comprising a respective hardwired-pipeline circuit that is coupled to receive and is operable in response to a respective clock signal that is unsynchronized with the respective clock signal received by at least one of the other hardwired-pipeline circuits. Referring, *e.g.,* to FIG. 6, Wong's Datapath Program Units (DPUs) 621a and 621b are clocked by a common signal distributed via the Clock Distribution bus 609. Consequently, the clock signals respectively received by the DPUs are synchronized, not unsynchronized like the clock signals recited in claim 1.

Furthermore, as the Applicants' attorney understands, Ebeling does not disclose the teaching missing from Wong, namely pipeline units each comprising a respective hardwired-pipeline circuit that is coupled to receive and is operable in response to a respective clock signal that is unsynchronized with the respective clock signal received by at least one of the other hardwired-pipeline circuits.

Claims 2-3, 5-7, and 9-10

These claims are patentable by virtue of their dependencies from claim 1.

Claim 11

Claim 11 as amended recites a pipeline bus coupled to a processor, to a configuration registry, and to a pipeline accelerator that includes a hardwired pipeline circuit, the pipeline bus operable to carry data between the processor and the pipeline accelerator and to carry hardwired-pipeline-configuration information from the registry to the pipeline accelerator.

For example, referring, to FIGS. 3-4 of the present patent application, a pipeline bus 50 is coupled to a host processor 42, to an accelerator-configuration registry 70 (via the host processor), and to a pipeline accelerator 44 that includes a hardwired pipeline circuit 80. The pipeline bus 50 is operable to carry data between the host processor 42 and the pipeline accelerator 44, and is operable to carry configuration information from the registry 70 to the pipeline accelerator, which uses the information to configure the hardwired pipeline circuit 80.

In contrast, Wong does not disclose a bus coupled to a processor, accelerator-configuration registry, and a pipeline accelerator, and operable to carry both data and configuration information. Referring, *e.g.,* to FIG. 16, col. 7, lines 30-35, col. 8, lines 15-16, and col. 8, lines 57-65, the bus between the ALU (processor) and the Adaptive Compute Module (ACM) carries data, but no configuration information. Instead, as best understood by the Applicants' attorney, one or more other busses carry configuration information from the Local Store Memory (LSM) (configuration registry) to the ACM to configure the DPUs (FIG. 6, hardwired-pipeline circuits) on the ACM. And even though the data bus between the ALU and ACM and the configuration busses from the LSM terminate at the ACM, there is not teaching or suggestion that the ACM couples the data bus to the configuration busses or otherwise to the LSM. Consequently, Wong discloses no single bus that corresponds to the pipeline bus recited in claim 11.

Furthermore, as the Applicants' attorney understands, Ebeling does not disclose the teaching missing from Wong, namely the pipeline bus recited in claim 11.

Claims 12-13

These claims are patentable by virtue of their dependencies from claim 11.

Claim 15

Claim 15 as amended is patentable for reasons similar to those recited above in support of the patentability of claim 1.

Claims 16-22

These claims are patentable by virtue of their dependencies from claim 15.

Claim 23

New claim 23 recites a processor operable to retrieve program instructions via a program-instruction bus, and a pipeline accelerator inoperable to communicate directly with the program-instruction bus.

Referring, e.g., to FIG. 3 of the present patent application, the pipeline bus 50 is inoperable to communicate directly with the program-instruction bus (the bus between the processing unit 62 and the processing-unit memory 66)

In contrast, referring, e.g., to column 8, lines 56-65, unlike the claimed pipeline accelerator, Wong's reconfigurable logic is operable to communicate directly with an instruction-interface bus.

And in contrast to the Examiner's assertion on p. 18, 3rd paragraph, the Applicants' attorney disagrees that Ebeling includes the teaching missing from Wong, namely a pipeline accelerator inoperable to communicate directly with a program-instruction bus. Referring to Ebeling's FIG. 8, as best understood by the Applicants' attorney, the instruction signals/bus 16 is operable to communicate directly with the configurable cells 26 via the control path 18. But even if Ebeling's bus 16 is inoperable to communicate directly with the cells 26, Ebeling's architecture is so different from Wong's architecture that there is no suggestion or motivation to combine the two architectures to obtain the computing machine recited in claim 23, nor is there a reasonable expectation of successfully obtaining a working architecture from such combination.

Claim 24

New claim 24 is patentable for reasons similar to those recited above in support of the patentability of claim 23.

Claims 25-27

These claims are patentable by virtue of their dependencies from claim 24.

New Claims 28 and 32-34

These claims are patentable by virtue of their dependencies on claim 11. Support for claim 28 is found, *e.g.,* in FIG. 3 of the patent application. Support for claims 33-34 re "application-specific integrated circuit" is found in, *e.g.*, paragraph [52] of the patent application, and support for claims 32 and 34 re 'field-programmable gate array" is found in original claim 4 of the patent application.

New Claims 29-31

These claims are patentable by virtue of their dependencies on claim 1. Support for claims 30-31 re "application-specific integrated circuit" is found in, *e.g.*, paragraph [52] of the patent application, and support for claims 29 and 31 re 'field-programmable gate array" is found in original claim 4 of the patent application.

CONCLUSION

In light of the foregoing, claims 2-3, 5-10, 12-14, and 16-27 as previously pending, claims 1, 4, 11, and 15 as amended, and new claims 28-34 are in condition for full allowance, and that action is respectfully requested.

In the event additional fees are due as a result of this amendment, you are hereby authorized to charge such payment to Deposit Account No. 07-1897.

DATED this 9th day of November, 2006.

Respectfully submitted,
GRAYBEAL JACKSON HALEY LLP

Bryan A. Santarelli
Attorney for Applicant
Registration No. 37,560
155-108th Avenue N.E., Ste 350
Bellevue, WA 98004-5973
(425) 455-5575